Schottky Junction Transistors for Micropower RFICs

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Abstract — **Results are presented from measurements and numerical simulations of Schottky Junction Transistors, a new type of micropower device capable of operating at GHz frequencies in the sub-threshold regime. Detailed measurements of the d.c. characteristics of a 2 μm gate length device agree well with numerical simulations. Measurements of transconductance and gate capacitance suggest that this relatively long gate length device will have a cut-off frequency of 126 MHz, which is again consistent with the numerical simulations. When projected to gate lengths of 0.1 μm, cut-off frequencies in excess of 10 GHz are predicted for drain currents of less than 1 μA/μm.**

I. Introduction

Micropower circuits, such as those used in digital watches and pacemakers, use a sub-threshold CMOS technology based on weakly inverted MOSFETs [1]. Although capable of very low power operation, these circuits are limited to operating frequencies below a few tens of MHz because of the relatively low cut-off frequency of a weakly inverted MOSFET. Below threshold, the maximum possible cut-off frequency of a MOSFET can be written as [2]

$$f_T = \mu U_T / 2\pi L_g^2 \qquad (1)$$

where U_T is the thermal voltage. The electron mobility in a weakly inverted MOSFET is μ~200 cm^2/Vs [3] and for a 2 μm gate length device we get f_T ~ 20 MHz. It is not practical to increase f_T by reducing the gate length because of problems with the transistor matching of sub-threshold MOSFETs [1]. For this reason, state-of-the-art micropower circuits typically use gate lengths L_g > 1 μm and operate at frequencies below 10 MHz [4] making them unsuitable for many RFIC applications.

We have recently proposed the Schottky Junction Transistor (SJT) as an alternative micropower device capable of operating at GHz frequencies [5]-[6]. The high cut-off frequency of the SJT is due to higher channel mobility, reduced gate capacitance and better transistor matching in the sub-threshold regime allowing for shorter gate length devices [6]. Here we present data from a 2 μm gate length SJT and show good agreement with the numerical simulations. When projected to gate lengths of 0.1 μm, cut-off frequencies in excess 20 GHz are anticipated. The high f_T values make SJTs ideally suited to micropower RFIC applications where power consumption is at a premium, including medical implants such as pacemakers and artificial cochlea.

II. Fabrication and Characterization

A cross-section through the SJT is shown in Fig. 1. The SOI channel thickness is 0.14 μm and it is doped n-type to a concentration of $6x10^{16}$ cm^{-3}. Device isolation is achieved by mesa etching down to the buried oxide (BOX) layer. Ohmic contacts are formed using spin-on-dopants and rapid thermal annealing. The gate is formed from $CoSi_2$ by depositing a cobalt layer and annealing at 750° C. During the anneal the silicide is formed by consuming the underlying silicon and the final channel thickness under the gate is 0.07 μm.

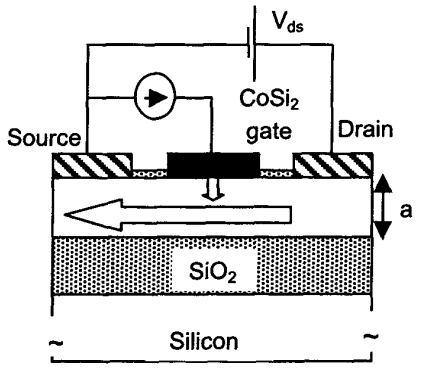

Fig. 1. Schematic cross-section of the SJT device showing the applied bias arrangement.

The SJT resembles a silicon-on-insulator (SOI) MESFET but its bias and operation is quite different. The channel doping and thickness are chosen such that the gate and drain currents both vary exponentially for small forward biases applied to the gate (V_{GS} < 0.3 V). Experimental results of the gate and drain currents from a 2 μm gate length device are shown in Fig. 2. Good agreement with the numerical simulations is obtained over

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the operating range of the device i.e for drain current in the range 1 nA to 1 μA as shown by the symbols. For the gate voltage range 0.05 to 0.25 V both I_D and I_G vary exponentially with an almost constant current gain. The SJT can therefore be operated as a current-controlled current-source similar to a bipolar junction transistor. The family of curves for the 2 μm SJT i.e. the drain current as a function of drain voltage for different gate currents is shown in Fig. 3. The low voltage for drain current saturation (~ $4U_T$) and high saturation impedance are characteristics of sub-threshold operation [1]-[2]. The data in Figs. 2 and 3 are the first measurements from a Schottky Junction Transistor.

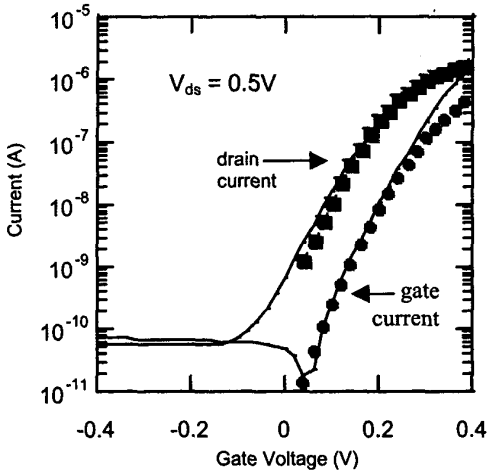

Fig. 2. The measured drain and gate currents as a function of gate voltage. The solid squares and circles represent the simulated values for the drain and gate currents respectively.

The d.c. current gain and transconductance are shown in Fig. 4 as a function of drain current. An analytical derivation of the current gain [5, 6] gives a constant value of

$$\beta = \frac{\varepsilon k^2 \mu}{a L_g^2 q^2 A^*} \frac{N_C}{N_D} \exp\left(\frac{qN_D a^2}{2\varepsilon U_T}\right) \qquad (2)$$

The current gain data in Fig. 4 is not a constant as predicted by (2) because of the different ideality factors for the drain and gate currents (*m* and *n* respectively). The value of β varies between 20 and 50 over a reasonable range of drain current.

The cut-off frequency of a transistor can be extracted from d.c. measurements of the transconductance, g_m, and gate capacitance, C_{gs}, i.e.

$$f_T = g_m / 2\pi C_{gs} \qquad (3)$$

A drain current of 10^{-7} A is close to the center of the operating range of the device (see Fig. 2) and at this value the measured transconductance is 2.7 x 10^{-6} S (see Fig 4.). We infer the input capacitance of the SJT from measurements made on somewhat larger Schottky diode structures processed under similar conditions to that of the SJT. At the gate bias of 0.17 V required for $I_d=10^{-7}$ A we measure a Schottky diode capacitance of 37 pF/cm^2 which would give C_{gs} = 3.4x10^{-15} F for the SJT gate. Substituting the values for C_{gs} and g_m in (3) gives f_T =126 MHz. This result compares very favorably to the value of 20 MHz expected for the 1 μm gate length weakly inverted MOSFET discussed above. Considerably higher values of f_T for shorter gate lengths are predicted from the simulations (see Section III below). We are confirming the cut-off frequency of the SJT by direct measurements of the high frequency s-parameters using devices with gate lengths in the range 0.5 to 0.1 μm.

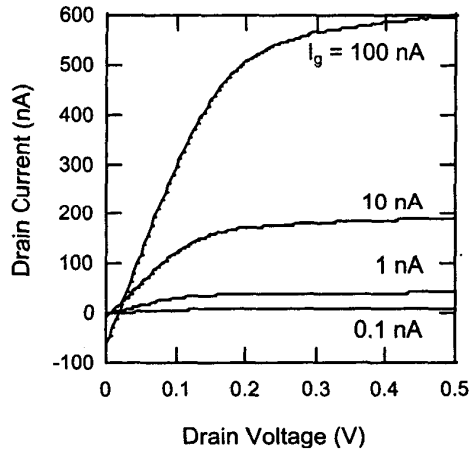

Fig. 3. The SJT family of curves (i.e. I_d vs V_{ds} for different I_g) for gate current bias in the range 0.1 to 100 na.

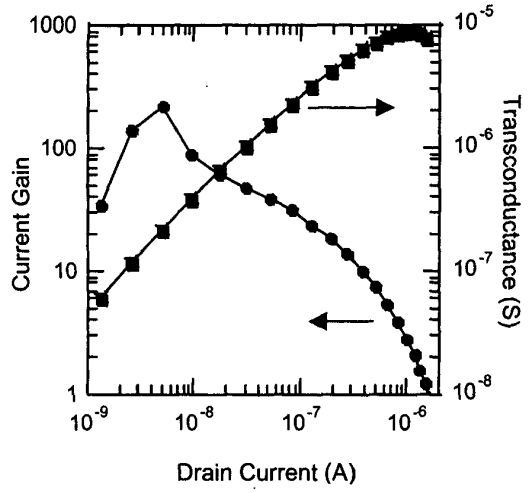

Fig. 4. The measured current gain (circles) and transconductance (squares) for the 2 μm gate length SJT. The drain voltage is 0.5 V.

III. Numerical Simulations

Numerical simulations of the SJT have been performed using the Atlas device simulator from Silvaco. Device parameters such as gate length (2.1 μm), channel width (4.2 μm), Schottky barrier height (0.64 eV), channel thickness (70 nm) and doping ($4x10^{16}$ cm^{-3}) are based on measured data. Other parameters such as interface trapped charged are more difficult to measure and are instead used as fitting parameters. The results from the numerical solutions (shown as solid symbols in Fig. 2) are derived assuming a positive oxide charge density of 1.3×10^{11} cm^{-2} at each $Si:SiO_2$ interface, which is a reasonable value for SIMOX SOI wafers [7]. The agreement with the measured drain and gate current is adequate, at least for the range of drain currents of interest.

We have used Atlas to extract the small-signal parameters of the SJT, thereby allowing us to derive the cut-off frequency. Results for different gate lengths in the range 1.0 to 0.3 μm are shown in Fig. 5. The solid line is a power-law fit to the data, extrapolated to gate lengths of 0.1 μm. The open circle is the value for the cut-off frequency of the 2 μm device, derived from the measurements presented above. The result from the measured device is consistent with the trend derived from the numerical simulations. This gives us some confidence that the numerical simulations accurately reflect the behavior of shorter gate length SJTs. The data in Fig. 5 suggests that deep sub-micron SJTs will have cut-off frequencies exceeding 10 GHz. This will make them ideally suited to micropower RFIC applications.

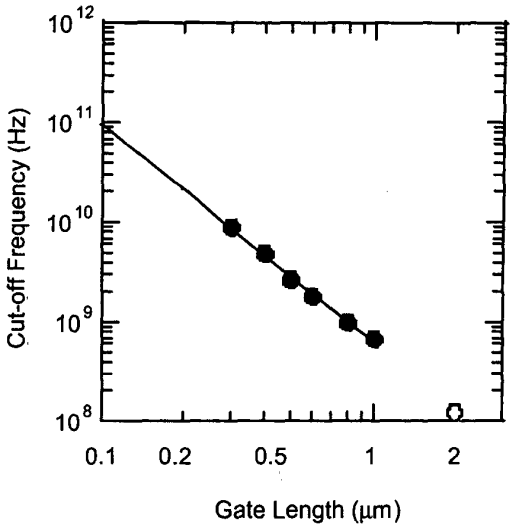

Fig. 5. Cut-off frequencies for different gate length SJTs. The solid circles are the results from numerical simulations. The open circle is the value derived from measurements of a 2 μm gate length device.

IV. Conclusions

We have presented the first d.c. measurements of a Schottky Junction Transistor, a novel micropower device capable of operating at GHz frequencies. The measurements confirm the very low power operating characteristics of the device. Numerical simulations of the transistor agree well with the measured data. Simulations of the small-signal parameters of the device suggest that cut-off frequencies in excess of 10 GHz will be possible for SJTs with gate lengths below 0.3 μm. The cut-off frequency for the 2 μm device is derived from the measured data and is consistent with the trend derived from the simulated devices. The value of f_T = 126 MHz is significantly higher than that expected for a weakly inverted MOSFET of similar geometry. We are currently extracting the cut-off frequencies of SJTs with gate lengths in the range 0.1 to 0.5 μm from s-parameter measurements.

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REFERENCES

[1] E. Vittoz in *Design of VLSI Circuits for Telecommunication and Signal Processing* 2e edited by J E Franca and Y Tsividis (Prentice Hall, 1994)

[2] Y Tsividis *Operation and Modeling of the MOS Transistor* 2e (McGraw-Hill, 1999)

[3] J T C Chen and R S Muller "Carrier Mobilities at Weakly Inverted Silicon Surfaces" *J. Appl. Phys.*, **45**, 828-834 (1974)

[4] C Toumazou, J Ngarmnil and T S Lande "Micropower log-domain-filter for Electronic Cochlea" *Electronics Letts*, **30**, 1839-1841 (1994)

[5] T J Thornton "The Schottky Junction Transistor: Micropower Circuits at GHz Frequencies" *IEEE Electron Dev. Letts* **22**, 38-40 (2001)

[6] T J Thornton "Physics and Applications of the Schottky Junction Transistor" *IEEE Trans. Electron Devices* **48**, 2421-2427 (2001)

[7] M A Pavenello and J A Martino "Extraction of the Oxide Charges at the Silicon Substrate Interface in Silicon-on-Insulator MOSFETS" *Solid State Electronics*, **43**, 2039-2046 (1999).